c2 Cancel

processor as data in a corresponding format according to the discrimination information; and

a data processor and converter processing the data stored in the memory unit.

REMARKS

Claims 1-36 are pending and under consideration and claims 2 and 20 have been amended as set forth above. Claims 1-36 stand rejected. No new matter is included in this Amendment.

Claim Objections

At page 2 of the Office Action, the Examiner objects to claim 2 because "predetermined code word and correction range" do not have an antecedent basis. Claim 2 has been amended as set forth above to correct the antecedent basis error noted by the Examiner.

The 35 U.S.C. §102(e) Rejection

At page 3 of the Office Action, claims 1, 4, 7, 11, 12, 14, 15 and 20-35 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,233,394 to Jeong et al. This rejection is respectfully traversed. Anticipation requires a disclosure in a single prior art reference of each and every element of the claimed invention, arranged as in the claim.

The Examiner asserts that Jeong et al. discloses a Phase Locked Loop (PLL) receiving two pulse streams to generate PLL clocks, referring particularly to Fig. 1, col. 2, lines 50-67 and col. 3, lines 1-39.

Fig. 1 illustrates a system decoder 200 having a connecting line to a digital phase locked loop 300, with the connecting line being annotated with Sf1 and Sf2. Col. 2, lines 54-58 read as follows:

> " A data stream, modulated by eight-to-sixteen modulation or eight-to-fourteen modulation (EFM/ESM) and shaped as a pulse wave, is transferred to a system decoder 200 which outputs control signals Sf1 and Sf2 to a phase locked loop (hereinafter referred to as a 'PLL') 300."

No mention is made at col. 2, line 54, through col. 3, line 39, nor elsewhere in Jeong et al. concerning the character of the control signals Sf1 and Sf2. Claim 1 recites "a PLL (Phase Locked Loop) to receive the pulse stream, to generate a PLL

clock." The "pulse stream" as recited in the body of claim 1 clearly refers to the "pulse stream of data from a DVD or a CD" as recited in the preamble of claim 1. There is no basis for concluding that the signals Sf1 and Sf2 are "a pulse stream of data from a DVD or a CD" as claimed in claim 1.

The Examiner asserts that Jeong et al. discloses a frame/ID sync detector to generate a symbol clock, referring to reference character 240. As shown in Fig. 2 and described at col. 4, lines 41-45, reference character 240 is a descrambler .

The Examiner asserts that Jeong et al. discloses a demodulator performing EFM+ in a DVD mode (212) and EFM in a CD mode (214). Admittedly, Jeong et al. includes features for demodulating both an ESM signal and an EFM signal. However, in Jeong et al., separate demodulators are used for ESM and EFM signals as indicated by the separate reference characters 212 and as described at col. 3, lines 44-46, "a switch 297 provides for separate DVD and CD processing according to a first disc identification signal disc 2 provided by the microcomputer (micro) 500." Thus, Jeong et al. fails to disclose "a demodulator [emphasis added] to EFM+ demodulate the pulse stream according to the symbol clock in a DVD mode, and [emphasis added] EFM demodulate the pulse stream according to the symbol clock in a CD mode, to generate demodulated data," as claimed in claim 1.

The Examiner asserts that Jeong et al. discloses [an] ECC (230, 235) to correct error according to a predetermined code length and error correction range and storing the data back into the memory, referring particularly to col. 4, lines 25-45. Col. 4, lines 25-27, of Jeong et al. disclose "[a] first error corrector 230 vertically and horizontally corrects errors in an error correction block of data read from a DVD system disc." Col. 4, lines 36-38 disclose "[a] second error correction means 235 corrects errors in data read from a CD system disc by using a conventional Cross Interleave Reed Soloman code." Just as in the demodulators, Jeong et al discloses the error correctors separately and thus does not disclose "an ECC [emphasis added] (error checking and correction) demodulator to error-correct the demodulated data stored in said memory according to a predetermined code length and error correction range, the predetermined code length and error correction range having different values in the DVD and CD modes," as claimed in claim 1.

Claims 4, 7, 11, 12, 14 and 15 are deemed to be patentable at least for similar reasons set forth above regarding claim 1.

Regarding claims 20-23, 25-29 and 31-35, the Examiner asserts that Jeong et al. discloses a single [emphasis added] preprocessor generating a clock from a pulse stream read from one of the DVD and the DC and performing demodulation according to the discrimination information, referring particularly to col. 3, lines 21-67 and col. 4, lines 1-3. Although independent claims 20, 25 and 31, recite "a signal [emphasis added] preprocessor" and not a "single [emphasis added] preprocessor" as stated by the Examiner, the Examiner correctly states that a feature of the present invention is an elimination of multiple processors to perform demodulation of various types of discs.

Claim 20 has been amended to recite "a signal pre-processor generating a clock from a pulse stream read from one of the DVD and the CD and performing demodulation of the pulse stream according to the discrimination information and the generated clock." As pointed out above regarding claim 1, Fig. 1 illustrates a system decoder 200 having a connecting line to a digital phase locked loop 300, with the connecting line being annotated with Sf1 and Sf2. As pointed out at col. 4, lines 4-7, of Jeong et al., the signals Sf are for controlling rotation of the disc 100 and not for generating a clock used for "performing demodulation of the pulse stream according to the discrimination information and the generated clock" as claimed in amended claim 20.

Claims 21-24 are deemed to be patentable at least for the reasons set forth above regarding claim 20.

Claims 25 and 31 recite "a signal pre-processor performing demodulation of the data according to the discrimination information." On the other hand, Jeong et al. discloses separate signal pre-processors, each performing demodulation of a specific type of signal and selecting one of the pre-processors to perform the demodulation based on a type of disc.

Claim 26 is deemed to be patentable at least for similar reasons set forth above regarding claim 20.

Claims 27-29 are deemed to be patentable at least for similar reasons set forth above regarding claims 25 and 26.

Claims 32-36 are deemed to be patentable at least for similar reasons set forth above regarding claims 25 and 26.

The First 35 U.S.C. §103(b) Rejection

At page 4 of the Office Action, claims 2-3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,233,394 to Jeong et al. in view of U.S. Patent 6,119,262 to Chang et al. This rejection is respectfully traversed.

Claims 2, 3 and 10 are deemed to be patentable at least for the reasons set forth above regarding claims 1 and 7.

The Second 35 U.S.C. §103(b) Rejection

At page 5 of the Office Action, claims 5-6, 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,233,394 to Jeong et al. in view of U.S. Patent 5,988,872 to Jeong.

Claims 5-6, 8 and 13 are deemed to be patentable at least for the reasons set forth above regarding claims 1, 7 and 12.

The Third 35 U.S.C. §103(b) Rejection

At page 6 of the Office Action, claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,233,394 to Jeong et al. in view of U.S. Patent 5,988,872 to Jeong and U.S. Patent 5,970,208 to Shim.

Claim 9 is deemed to be patentable at least for the reasons set forth above regarding claim 7.

The Fourth 35 U.S.C. §103(b) Rejection

At page 6 of the Office Action, claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,233,394 to Jeong et al. in view of U.S. Patent 6,119,262 to Chang et al.

Claims 16-19 are deemed to be patentable at least for the reasons set forth above regarding claim 1.

Summary

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 6/4/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please AMEND the following claims:

2. (ONCE AMENDED) The combined DVD/CD data processor as claimed in claim 1, wherein the predetermined code [word] length and error correction range in the DVD mode are PI(182,172), PO(208,192), and the predetermined code [word] length and error correction range in the CD mode are C1(32,28), C2(28,24).

20. (ONCE AMENDED) A data processor apparatus for common use in a DVD (Digital Video Disk)/CD (Compact Disk) player using discrimination information provided according to a DVD or a CD, comprising:

a signal pre-processor generating a clock from a pulse stream read from one of the DVD and the CD and performing demodulation of the pulse stream according to the discrimination information and the generated clock;

a memory unit storing the demodulated pulse stream processed by the signal pre-processor as data in a corresponding format according to the discrimination information; and

a data processor and converter processing the data stored in the memory unit.